ACADEMIC REGULATIONS, COURSE STRUCTURE

AND

COURSE STRUCTURE

HITS R22

M.Tech – Embedded Systems

M.Tech - Regular Two Year Degree Programme
(For batches admitted from the academic year 2022 - 2023)

Holy Mary Institute of Technology & Science
Bogaram (V), Keesara (M), Medchal (Dist) - 501 301

FOREWORD

The autonomy is conferred on Holy Mary Institute of Technology & Science by UGC based on its performance as well as future commitment and competency to impart quality education. It is a mark of its ability to function independently in accordance with the set norms of the monitoring bodies like UGC and AICTE. It reflects the confidence of the UGC in the autonomous institution to uphold and maintain standards it expects to deliver on its own behalf and thus awards degrees on behalf of the college. Thus, an autonomous institution is given the freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

Holy Mary Institute of Technology & Science is proud to win the credence of all the above bodies monitoring the quality in education and has gladly accepted the responsibility of sustaining, if not improving upon the standards and ethics for which it has been striving for more than a two decades in reaching its present standing in the arena of contemporary technical education. As a follow up, statutory bodies like Academic Council and Boards of Studies are constituted with the guidance of the Governing Body of the College and recommendations of the JNTU Hyderabad to frame the regulations, course structure and syllabi under autonomous status.

The autonomous regulations, course structure and syllabi have been prepared after prolonged and detailed interaction with several expertise solicited from academics, industry and research, in accordance with the vision and mission of the college to order to produce quality engineering graduates to the society.

All the faculty, parents and students are requested to go through all the rules and regulations carefully. Any clarifications, if needed, are to be sought, at appropriate time and with principal of the college, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The Cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the college and brighter prospects of engineering graduates.

PRINCIPAL

ACADEMIC REGULATIONS

M. Tech. - Regular Two Year Degree Programme
(For batches admitted from the academic year 2022 - 23)

For pursuing two year post graduate Masters Degree Programme of study in Engineering (M.Tech) offered by Holy Mary Institute of Technology & Science under Autonomous status and herein referred to as HITS (Autonomous):

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2022-23 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for Holy Mary Institute of Technology & Science (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Holy Mary Institute of Technology & Science shall be the Chairman, Academic Council.

1. ADMISSION

Admission into first year of two year M. Tech. degree Program of study in Engineering:

Eligibility:

Admission to the above programme shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt., From time to time.

The medium of instructions for the entire post graduate programme in Engineering & technology will be English only.

2. AWARD OF M. Tech. DEGREE

A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after two academic years of course work, failing which he shall forfeit his seat in M. Tech. programme.

The student shall register for all **68** credits and secure all the **68** credits.

The minimum instruction days in each semester are 90.

3. BRANCH OF STUDY

The following specializations are offered at present for the M. Tech programme of study.

1. Highway Engineering
2. CSE
3. Computer Networks & Information Security
4. Embedded Systems
5. VLSI Design
6. Electrical Power Systems
7. Power Electronics
8. CAD / CAM
9. Machine Design

4. COURSE REGISTRATION

4.1 A 'Faculty Advisor or Counselor' shall be assigned to each student, who will advise him on the Post Graduate Programme (PGP), its Course Structure and Curriculum, Choice / Option for Courses, based on his competence, progress, pre-requisites and interest.

4.2 Academic Section of the College invites 'Registration Forms' from students within 15 days from the commencement of class work, ensuring 'DATE and TIME Stamping'. The Registration Requests for any 'CURRENT SEMESTER' shall be completed BEFORE the commencement of SEEs (Semester End Examinations) of the 'PRECEDING SEMESTER'.

4.3 A Student can apply Registration, ONLY AFTER obtaining the 'WRITTEN APPROVAL' from his Faculty Advisor, which should be submitted to the College Academic Section through the Head of Department (a copy of it being retained with Head of Department, Faculty Advisor and the Student).

4.4 If the Student submits ambiguous choices or multiple options or erroneous entries - during Registration for the Course(s) under a given/ specified Course Group/ Category as listed in the Course Structure, only the first mentioned Course in that Category will be taken into consideration.

4.5 Course Registrations are final and CANNOT be changed, nor can they be inter-changed; further, alternate choices will also not be considered. However, if the Course that has already been listed for Registration (by the Head of Department) in a Semester could not be offered due to any unforeseen or unexpected reasons, then the Student shall be allowed to have alternate choice - either for a new course (subject to offering of such a course), or for another existing course (subject to availability of seats), which may be considered. Such alternate arrangements will be made by the Head of Department, with due notification and time-framed schedule, within the FIRST WEEK from the commencement of Class-work for that Semester.

5. ATTENDANCE

The programmes are offered on a unit basis with each subject being considered a unit.

5.1 Attendance in all classes (Lectures/Laboratories etc.) is compulsory. The minimum required attendance in each theory / Laboratory etc. is 75% including the days of attendance in sports, games, NCC and NSS activities for appearing for the End Semester examination. A student shall not be permitted to appear for the Semester End Examinations (SEE) if his attendance is less than 75%.

5.2 Condonation of shortage of attendance in each subject up to 10% (65% and above and below75%) in each semester shall be granted by the College Academic Committee.

5.3 Shortage of Attendance below 65% in each subject shall not be condoned.

5.4 Students whose shortage of attendance is not condoned in any subject are not eligible to write their end semester examination of that subject and their registration shall stand cancelled.

5.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

5.6 A Candidate shall put in a minimum required attendance at least three (3) theory courses in I Year I semester for promoting to I Year II Semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the courses, as per the course structure.

5.7 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present Semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission in to the same class.

6. ACADEMIC REQUIREMENTS

The following academic requirements must be satisfied, in addition to the attendance requirements mentioned in item no. 5. The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks per subject / course (theory / practical), based on Internal Evaluation and Semester End Examination.

6.1 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course, if he secures not less than:

- 40% of Marks (24 out of 60 marks) in the Semester End Examination;
- 40% of Marks in the internal examinations (16 out of 40 marks allotted for CIE); and A minimum of 50% of marks in the sum total of CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades this implies securing **'B'** Grade or above in a subject.

6.2 A student shall register for all subjects for total of **68** credits as specified and listed in the course structure for the chosen specialization, put in the required attendance and fulfill the academic requirements for securing **68** credits obtaining a minimum of 'B' Grade or above in each subject, and all **68** credits securing Semester Grade Point Average **(SGPA)**

- **6.0** (in each semester) and final Cumulative Grade Point Average **(CGPA)** (i.e., CGPA at the end of PGP**)**
- **6.0**, and shall ***pass all the mandatory Audit Courses*** to complete the PGP successfully.

Note: (1) The SGPA will be computed and printed on the marks memo only if the candidate passes in all the subjects offered and gets minimum B grade in all the subjects.

(2) CGPA is calculated only when the candidate passes in all the subjects offered in all the Semesters.

6.3 A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to Mini Project with seminar, if student secures not less than 50% marks (i.e. 50 out of 100 allotted marks). The student would be treated as failed, if student (i) does not submit a seminar report on Mini Project or does not make a presentation of the same before the evaluation committee as per schedule or (ii) secures less than 50% marks in Mini Project with seminar evaluation. The failed student shall reappear for the above evaluation when the notification for supplementary examination is issued.

6.4 A candidate shall be deemed to have secured the minimum academic requirement in a Course if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

6.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.1) he has to re appear for the Semester End Examination in that course.

6.6 A candidate shall be given one chance to re-register for the courses if the internal marks secured by a candidate is less than 50% and failed in that course for maximum of two courses and should register within four weeks of commencement of the class work. In such a case, the candidate must re-register for the courses and secure the required minimum attendance. The candidate's attendance in the re-registered course(s) shall be calculated separately to decide upon his eligibility for writing the Semester End Examination in those courses. In the event of the student taking another chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stands cancelled.

6.7 In case the candidate secures less than the required attendance in any course, he shall not be permitted to write the Semester End Examination in that course. He shall re-register for the course when next offered.

6.8 Offering one open elective courses in III-Semester along with core and specialized courses as a part of inculcating knowledge to the student.

7. EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

Continuous Internal Evaluation (CIE)

The performance of a student in each semester shall be evaluated subject- wise (irrespective of credits assigned) for a maximum of 100 marks.

7.1 The performance of a student in every subject/course (including practical's and Project) will be Evaluated for 100 marks each, with 40 marks allotted for CIE (Continuous Internal Evaluation) and 60 marks for SEE (Semester End-Examination). The Continuous Internal Evaluation shall be made based on the average of the marks secured in the two Mid-Term Examinations conducted, first Mid-Term examinations in the middle of the Semester and second Mid-Term examinations during the last week of instruction.

7.1.1 **Continuous Internal Evaluation:**

In CIE, for theory subjects, during a semester, there shall be two mid-term examinations. Each Mid-Term examination consists of two parts,

i) Part – A for 10 marks,

- ✓ Part - A: Objective/quiz paper for 10 marks. (The objective/quiz paper is set with multiple choice, fill-in the blanks and match the following type of questions for a total of 10 marks.)

ii) Part – B for 20 marks with a total duration of 2 hours as follows:

- ✓ Part - B : Descriptive paper for 20 marks (The descriptive paper shall contain 6 full questions out of which, the student has to answer 4 questions, each carrying 5 marks.)

iii) **The remaining 10 marks of Continuous Internal Evaluation are distributed as**

a) Assignment for 5 marks (Average of 2 Assignments each for 5 marks)

b) Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks

7.1.2 While the first mid-term examination shall be conducted on 50% of the syllabus, the second mid-term examination shall be conducted on the remaining 50% of the syllabus.

Five (5) marks are allocated for assignments (as specified by the subject teacher concerned). The first assignment should be submitted before the conduct of the first mid-term examination, and the second assignment should be submitted before the conduct of the second mid-term examination. The average of the two assignments shall be taken as the final marks for assignment (for 5 marks).

Subject Viva-Voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject for 5 marks before II Mid-Term Examination.

7.1.3 The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

The details of the end semester question paper pattern are as follows:

Semester End Examination (SEE):

The Semester End Examinations (SEE), for theory subjects, will be conducted for 60 marks consisting of two parts viz. i) Part- A for 10 marks, ii) Part - B for 50 marks.

- Part-A is a compulsory question which consists of ten sub-questions from all units carrying equal marks.
- Part-B consists of five questions (numbered from 2 to 6) carrying 10 marks each. Each of these Questions is from each unit and may contain sub-questions. For each question there will be an "either" "or" choice, which means that there will be two questions from each unit and the student should answer either of the two questions.
- The duration of Semester End Examination is 3 hours.

7.2 For practical subjects there shall be a Continuous Internal Evaluation (CIE) during the semester for 40 marks and 60 marks for semester end examination. Out of the 40 marks for internal evaluation:

1. A write-up on day-to-day experiment in the laboratory (in terms of aim, components/procedure, expected outcome) which shall be evaluated for 10 marks
2. 10 marks for viva-voce (or) tutorial (or) case study (or) application (or) poster presentation of the course concerned.
3. Internal practical examination conducted by the laboratory teacher concerned shall be evaluated for 10 marks.
4. The remaining 10 marks are for Laboratory Project, which consists of the Design (or) Software /Hardware Model Presentation (or) App Development (or) Prototype Presentation submission which shall be evaluated after completion of laboratory course and before semester end practical examination.

7.3 The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the cluster / other colleges which will be decided by the examination branch of the institution.

In the Semester End Examination, held for 3 hours, total 60 marks are divided and allocated as shown below:

1. 10 marks for write-up
2. 15 for experiment/program
3. 15 for evaluation of results
4. 10 marks for presentation on another experiment/program in the same laboratory course
5. 10 marks for viva-voce on concerned laboratory course.

The Student, in each subject, shall have to earn 40% of marks (i.e. 16 marks out of 40 marks) in CIE, 40% of marks (i.e. 24 marks out of 60) in SEE and Overall 50% of marks (i.e. 50 marks out of 100 marks) both CIE and SEE marks taking together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

For conducting laboratory end examinations of all PG Programmes, one internal examiner and one external examiner are to be appointed by the Chief Controller of Examination in one week before for commencement of the lab end examinations.

7.4 A candidate shall be deemed to have secured the minimum academic requirement in a Course if he secures a minimum of 40% of marks in the Semester End Examination and a minimum aggregate of 50% of the total marks in the Semester End Examination and Continuous Internal Evaluation taken together.

7.5 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 6) he has to re appear for the Semester End Examination in that course.

8. RE-ADMISSION/RE-REGISTRATION

8.1 **Re-Admission for Discontinued Student:** A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for '**readmission**' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned, subject to item 5.1.

8.2 If a student is detained in a subject (s) due to shortage of attendance in any semester, he may be permitted to **re-register** for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he seeks re-registration, with prior permission from the authorities concerned, subject to item 6.2.

8.3 ***A candidate shall be given only one-time chance to re-register and attend the classes for a maximum of two subjects in a semester***, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

9. EXAMINATIONS AND ASSESSMENT - THE GRADING SYSTEM

9.1 Marks will be awarded to indicate the performance of each student in each Theory Course, or Lab/ Practicals, or Seminar, or Project, etc., based on the % marks obtained in CIE + SEE (Continuous Internal Evaluation + Semester End Examination, both taken together) as specified in Item6above, and a corresponding Letter Grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed:

% of Marks Secured (Class Intervals)	***Letter Grade (UGC Guidelines)***	***Grade Points***
90% and above (≥ 90% , ≤ 100%)	O (Outstanding)	10
Below 90% but not less than 80% (≥ 80% , < 90%)	A^+ (Excellent)	9
Below 80% but not less than 70% (≥ 70% , < 80%)	A (Very Good)	8
Below 70% but not less than 60% (≥ 60% , < 70%)	B^+ (Good)	7
Below 60% but not less than 50% (≥ 50% , < 60%)	B (above Average)	6
Below 50% (< 50%)	F (FAIL)	0
Absent	AB	0

9.3 A student obtaining F Grade in any Course shall be considered 'failed' and is be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered. In such cases, his Internal Marks (CIE Marks) in those Courses will remain the same as those he obtained earlier.

9.4 A student not appeared for examination then 'AB' Grade will be allocated in any Course shall be considered 'failed' and will be required to reappear as 'Supplementary Candidate' in the Semester End Examination (SEE), as and when offered.

9.5 A Letter Grade does not imply any specific Marks percentage and it will be the range of marks percentage.

9.6 In general, a student shall not be permitted to repeat any Course(s) only for the sake of 'Grade Improvement' or 'SGPA / CGPA Improvement'.

9.7 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course. The corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Subject / Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.8 The Student passes the Course only when he **gets GP>=6 (B Grade or above).**

9.9 A student earns Grade Point (GP) in each Course, on the basis of the Letter Grade obtained by him in that Course (excluding Mandatory non-credit Courses). Then the corresponding 'Credit Points' (CP) are computed by multiplying the Grade Point with Credits for that particular Course.

Credit Points (CP) = Grade Point (GP) x Credits …. For a Course

9.10 The Semester Grade Point Average (SGPA) is calculated by dividing the Sum of Credit Points (ΣCP)secured from ALL Courses registered in a Semester, by the Total Number of Credits registered during that Semester. SGPA is rounded off to TWO Decimal Places. SGPA is thus computed as

SGPA = $\{\sum_{i=1}^{N} C_i\ G_i\}$ / $\{\sum_{i=1}^{N} C_i\}$ …. For each Semester,

where 'i' is the Course indicator index (takes into account all Courses in a Semester), 'N' is the no. of Courses 'REGISTERED' for the Semester (as specifically required and listed under the Course Structure of the parent Department), C_i is the no. of Credits allotted to that ix Course, and G_i represents the Grade Points (GP) corresponding to the Letter Grade awarded for that its Course.

Illustration of Computation of SGPA

Course	Credit	Grade Letter	Grade Point	Credit Point (Credit x Grade)
Course1	3	A	8	3 x 8 = 24
Course2	3	B+	7	4 x 7 = 28
Course3	3	B	6	3 x 6 = 18
Course4	3	O	10	3 x10= 30
Course5	3	C	5	3 x 5 = 15
Course6	3	B	6	4 x 6 = 24

Thus, **SGPA =139/18 =7.72**

9.11 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all Semesters considered for registration. The CGPA is the ratio of the Total Credit Points secured by a student in ALL registered Courses in ALL Semesters, and the Total Number of Credits registered in ALL the Semesters. CGPA is rounded off to

TWO Decimal Places. CGPA is thus computed from the I Year Second Semester onwards, at the end of each Semester, as per the formula

$$CGPA = \{ \sum_{j=1}^{M} C_j G_j \} / \{ \sum_{j=1}^{M} C_j \} \ldots \quad \text{for all S Semesters registered}$$

(i.e., up to and inclusive of S Semesters, S ≥ 2)

where 'M' is the TOTAL no. of Courses (as specifically required and listed under the Course Structure of the parent Department) the Student has 'REGISTERED' from the 1st Semester onwards up to and inclusive of the Semester S (obviously M > N), 'j' is the Course indicator index (takes into account all Courses from 1 to S Semesters), C_j is the no. of Credits allotted to the jth Course, and G_j represents the Grade Points (GP) corresponding to the Letter Grade awarded for that jth Course. After registration and completion of I Year I Semester however, the SGPA of that Semester itself may be taken as the CGPA, as there are no cumulative effects.

For CGPA Computation

Semester 1	Semester 2	Semester 3	Semester 4
Credits : 18 SGPA : 7.72	Credits : 18 SGPA : 7.8	Credits : 12 SGPA : 5.6	Credits : 20 SGPA : 6.0

Thus, **CGPA =** $\dfrac{18 \times 7.72 + 18 \times 7.8 + 12 \times 5.6 + 20 \times 6.0}{68} = 6.86$

9.12 For Calculations listed in Item 9.6 – 9.11, performance in failed Courses (securing F Grade) will also be taken into account, and the Credits of such Courses will also be included in the multiplications and summations.

9.13 No SGPA/CGPA is declared, if a candidate is failed in any one of the courses of a given semester.

9.14 Conversion formula for the conversion of GPA into indicative percentage is

% of marks scored = (final CGPA -0.50) x 10

10 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

10.1 A Project Review Committee (PRC) shall be constituted with Head of the Department as Chairperson, Project Supervisor and one senior faculty member of the Departments offering the M. Tech. programme.

10.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical.

10.3 After satisfying 10.2, a candidate has to submit, in consultation with his Project Supervisor, the title, objective and plan of action of his project work to the PRC for approval. Only after obtaining the approval of the PRC the student can initiate the Project work.

10.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

10.5 A candidate shall submit his project status report in two stages at least with a gap of three months between them.

10.6 The work on the project shall be initiated at the beginning of the II year and the duration of

the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of all theory and practical courses with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.

10.7 After approval from the PRC, the soft copy of the thesis should be submitted to the College for **ANTI-PLAGIARISM** for the quality check and the plagiarism report should be included in the final thesis. If the copied information is less than **30%**, then only thesis will be accepted for submission.

10.8 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College.

10.9 For **Dissertation work Review-I** in II Year I Sem. there is an internal marks of 100, the evaluation should be done by the PRC for 50 marks and Supervisor will evaluate for 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work and Literature Survey in the same domain. A candidate has to secure a minimum of 50% of marks to be declared successful for Project Phase-I. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

10.10 *For **Dissertation Work Review - II*** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the DRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The DRC will examine the overall progress of the Dissertation Work and decide whether or not the Dissertation is eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he fails to obtain the required minimum marks, he has to reappear for Dissertation Work Review - II as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate has to secure a minimum of 50% marks in Dissertation Evaluation (Viva-Voce) examination.

10.11 Dissertation Work Reviews - I and II shall be conducted in phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - II (Phase I). These students shall reappear for Dissertation Work Review - II in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - I, and then Dissertation Work Review - II follows. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for Dissertation Work Review – II in the next academic year only at the time of Dissertation Work Review - II (Phase I).

10.12 If he fails to fulfill as specified in 10.10, he will reappear for the Viva-Voce examination only after three months. In the reappeared examination also, fails to fulfill, he will not be eligible for the award of the degree.

10.13 The thesis shall be adjudicated by one examiner selected by the Chief Controller of Examinations. For this, the HOD of the Department shall submit a panel of 3 examiners, eminent in that field, with the help of the guide concerned and Head of the Department.

10.14 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

10.15 If the report of the examiner is favorable, Project dissertation shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis.

10.16 The Head of the Department shall coordinate and make arrangements for the conduct of Project dissertation.

10.17 For mandatory non-credit Audit courses, a student has to secure 40 marks out of 100 marks (i.e.40% of the marks allotted) in the continuous internal evaluation for passing the subject/course. These marks should also be uploaded along with the internal marks of other subjects. No marks or Letter Grade shall be allotted for these courses/activities. However, for non-credit courses '**SATISFACTORY'** or "**UNSATISFACTORY'** shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA.

11. AWARD OF DEGREE AND CLASS

11.1 A Student who registers for all the specified Courses/ Courses as listed in the Course Structure, satisfies all the Course Requirements, and passes the examinations prescribed in the entire PG Programme (PGP), and secures the required number of 68 Credits (with CGPA ≥ 6.0), shall be declared to have 'QUALIFIED' for the award of the M.Tech. Degree in the chosen Branch of Engineering and Technology with specialization as he admitted.

11.2 **Award of Class**

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes based on the CGPA:

Class Awarded	Grade to be Secured
First Class with Distinction	CGPA ≥ 7.75
First Class	6.75 to < 7.75 CGPA
Second Class	6.00 to < 6.75 CGPA

11.3 A student with final CGPA (at the end of the PGP) < 6.00 will not be eligible for the Award of Degree.

12. WITHOLDING OF RESULTS

If the student has not paid the dues, if any, to the college or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

13. TRANSITORY REGULATIONS

13.1 If any candidate is detained due to shortage of attendance in one or more courses, they are eligible for re-registration to maximum of two earlier or equivalent courses at a time as and when offered.

13.2 The candidate who fails in any course will be given two chances to pass the same course; otherwise, he has to identify an equivalent course as per HITS21 Academic Regulations.

14. SUPPLEMENTARY EXAMINATIONS

Supplementary examinations for the odd semester shall be conducted with the regular examinations of even semester and vice versa, for those who appeared and failed or absent in regular examinations. Such candidates writing supplementary examinations may have to write more than one examination.

15. REVALUATION

Students shall be permitted for revaluation after the declaration of end semester examination results within due dates by paying prescribed fee. After revaluation if there is any betterment in the grade, then improved grade will be considered. Otherwise old grade shall be retained.

16. AMENDMENTS TO REGULATIONS

The Academic Council of Holy Mary Institute of Technology & Science reserves the right to revise, amend, or change the regulations, scheme of examinations, and / or syllabi or any other policy relevant to the needs of the society or industrial requirements etc., without prior notice.

17. GENERAL

17.1 **Credit**: A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (lecture or tutorial) or two hours of practical work/field work per week.

17.2 **Credit Point:** It is the product of grade point and number of credits for a course.

17.3 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”.

17.4 The academic regulation should be read as a whole for the purpose of any interpretation.

17.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

Malpractices Rules - Disciplinary Action For /Improper Conduct in Examinations

S. No	Nature of Malpractices / Improper Conduct	Punishment
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the course of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the course of the examination)	Expulsion from the examination hall and cancellation of the performance in that course only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that course only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the course of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the courses of that Semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the courses of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that course.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that course and all other courses the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the courses of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that course and all the other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is course to the academic regulations in connection with forfeiture of seat.

8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that course and all other courses the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the courses of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that course and all other courses the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

COURSE STRUCTURE

M.Tech – Embedded Systems

I Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B2ES101PC	Digital System Design with FPGAs	PC	3	-	-	3	40	60	100
B2ES102PC	System Design with Embedded Linux	PC	3	-	-	3	40	60	100
B2ES103PC	Research Methodology and IPR	PC	2	-	-	2	40	60	100
	Professional Elective - I	PE	3	-	-	3	40	60	100
	Professional Elective - II	PE	3	-	-	3	40	60	100
B2ES104PC	Digital System Design with FPGAs Lab	PC	-	-	4	2	40	60	100
B2ES105PC	System Design with Embedded Linux Lab	PC	-	-	4	2	40	60	100
	Total		**14**	**-**	**8**	**18**	**280**	**420**	**700**
Audit Course(Non Credit)									
	Audit Course – I	AC	2	-	-	-	100	-	100

II Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B2ES201PC	ARM Microcontrollers	PC	3	-	-	3	40	60	100
B2ES202PC	Digital Control Systems	PC	3	-	-	3	40	60	100
	Professional Elective – III	PE	3	-	-	3	40	60	100
	Professional Elective – IV	PE	3	-	-	3	40	60	100
B2ES204PC	ARM Microcontrollers Lab	PC	-	-	4	2	40	60	100
B2ES205PC	Digital Control Systems Lab	PC	-	-	4	2	40	60	100
B2ES201PW	Mini Project with Seminar	PWC			4	2	100	-	100
	Total		**12**	**-**	**12**	**18**	**340**	**360**	**700**
Audit Course(Non Credit)									
	Audit Course – II	AC	2	-	-	-	100	-	100

III Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
	Professional Elective - V	PE	3	-	-	3	40	60	100
	Open Elective	OE	3	-	-	3	40	60	100
B2ES302PW	Dissertation Phase - I	PWC	-	-	12	6	100	-	100
	Total		**6**	**-**	**12**	**12**	**180**	**120**	**300**

IV Semester									
Course Code	Course Title	Category	Hours per Week			Credits	Scheme of Examination Maximum Marks		
			L	T	P		CIE	SEE	Total
B2ES403PW	Dissertation Phase - II	PWC	-	-	12	06	100	-	100
B2ES404PW	Dissertation Viva Voce	PWC	-	-	28	14	-	100	100
	TOTAL		**-**	**-**	**40**	**20**	**100**	**100**	**200**

Total Credits = 68

PROFESSIONAL ELECTIVES			
PE- I		PE – II	
B2ES101PE	Programming Languages for Embedded Software	B2ES104PE	Communications Buses & Interfaces
B2ES102PE	AI & Machine Leaning	B2ES105PE	Parallel Processing
B2ES103PE	Computer Vision	B2ES106PE	Advanced Computer architecture
PE – III		PE – IV	
B2ES207PE	IOT & Applications	B2ES210PE	Hardware Software Co-Design
B2ES208PE	VLSI Signal Processing	B2ES211PE	Network Security and Cryptography
B2ES209PE	SOC Architecture	B2ES212PE	Physical Design Automation
PE – V			
B2ES313PE	Scripting Languages		
B2ES314PE	Memory Technologies		
B2ES315PE	Wireless Sensor Networks		

OPEN ELECTIVES	
B2ES401OE	Artificial Neural Networks
B2ES402OE	Internet of Things
B2ES403OE	Adhoc & Sensor Networks
B2ES404OE	Information Retrieval Systems

AUDIT COURSE I		AUDIT COURSE II	
B2ES101AC	English for Research Paper Writing	B2ES203AC	Disaster Management
B2ES102AC	Pedagogy Studies	B2ES204AC	Personality Development through Life Enrichment Skills

I YEAR (I-SEMESTER)

DIGITAL SYSTEM DESIGN WITH FPGAs

I-M.Tech I Semester **L T P C**
Course Code:B2ES101PC **3 0 0 3**

Pre-Requisite: Switching Theory and Logic Design

COURSE OBJECTIVES:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an over view of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

COURSE OUTCOMES:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT-I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB an slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1,ACT2and ACT3 Architectures.

UNIT-II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design strategies for multi-clock sequential circuits

UNIT-III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Over view of computer Aided Design

UNIT-IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT-V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

TEXT BOOKS:

1. Digital Electronics and design with VHDL – Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design – Charles H.Roth, Jr.- 5th Ed., Cengage Learning.

REFERENCE BOOKS:

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices-Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory- Zvi Kohavi & NirajK. Jha, 3rd Edition, Cambridge, 2010.

SYSTEM DESIGN WITH EMBEDDED LINUX

I-M.Tech I Semester **L T P C**
Course Code: B2ES102PC **3 0 0 3**

COURSE OBJECTIVES:

1. To understand and make effective use of Linux utilities and Shell scripting language (bash) to solve Problems.
2. To implement in C some standard Linux utilities such as ls, mv, cp etc. using system calls.
3. To develop the skills necessary for systems programming including files system programming, process and signal management, and inter process communication

COURSE OUTCOMES: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Understand and create Linux BSP for a hardware platform

UNIT-I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling.
Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT-II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking sub system, IPC, User space, Start-up sequence

UNIT-III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2C,USB,Timer,KernelModules

UNIT-IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT-V

Building and Debugging: Boot loaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds “Mastering Embedded Linux Programming ”-Second Edition, PACKT Publications Limited.
2. KarimYaghmour, “Building Imbedded Linux Systems”, O 'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, “Embedded Linux System Design and Development”,Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, “Embedded Linux Primer: A practical Real World Approach”, Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wey, 1st Edition, 2014

RESEARCH METHODOLOGY AND IPR

I-M.Tech I Semester **L T P C**
Course Code:B2ES103PC **2 0 0 2**

COURSE OBJECTIVES:

1. To understand the research problem
2. To know the literature studies, plagiarism and ethics
3. To get the knowledge about technical writing
4. To analyze the nature of intellectual property rights and new developments
5. To know the patent rights

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

UNIT-II

Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT-III

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT-IV

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development.
International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT

UNIT-V

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR,IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard," Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, “Research Methodology: A step by Step Guide for beginners”
2. Halbert, “ Resisting Intellectual Property”, Taylor & FrancisLtd,2007.
3. Mayall, “Industrial Design”, McGraw Hill, 1992.
4. Niebel, “Product Design”, McGraw Hill, 1974.
5. Asimov, “Introduction to Design”, Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
7. T. Ramappa, “Intellectual Property Rights Under WTO”,S. Chand,2008

PROGRAMMING LANGUAGE FOR EMBEDDED SOFTWARE
(Professional Elective-1)

I-M.Tech I Semester **L T P C**
Course Code:B2ES101PE **3 0 0 3**

COURSE OBJECTIVES:
1. To develop skills in embedded system programming
2. To provide the ability of identifying the choice of programming language for embedded systems
3. To differentiate interpreted languages from compiled languages.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Write an embedded C application of moderate complexity.
2. Develop and analyze algorithms in C++.
3. Differentiate interpreted languages from compiled languages.

UNIT–I
Embedded 'C' Programming
- Bit wise operations, Dynamic memory allocation, OS services
- Linked stack and queue, Sparse matrices, Binary tree
- Interrupt handling in C, Code optimization issues
- Writing LCD drives, LED drivers, Drivers for serial port communication
- Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT–II
CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods ,'this' pointer, constructors, destructors, friend function ,dynamic memory allocation

UNIT–III
Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT–IV
Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions.

UNIT–V
Scripting Languages Overview of Scripting Languages–PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

TEXT BOOKS:
1. Michael J. Pont, " Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O' Reilly Publications, 6th Edition 2011

REFERENCE BOOKS:
1. A. Michael Berman, "Data structures via C++" , Oxford University Press, 2002
2. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005

ARTIFICIAL INTELLIGENCE & MACHINE LEARNING
(Professional Elective-1)

I-M.Tech I Semester **L T P C**
Course Code:B2ES102PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce students to the basic concepts and techniques of Machine Learning.
2. To develop skills of using recent machine learning's of tware for solving practical problems.
3. To gain experience of doing independent study and research.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Apply the basic principles, models, and algorithms of AI in different solutions
2. Recognize, model, and solve problems in the analysis and design of information systems.
3. Analyze the structures and algorithms of a selection of techniques related to searching, reasoning, machine learning, and language processing.

UNIT–I
Supervised Learning (Regression/Classification)
Basic methods: Distance-based methods, Nearest-Neighbors, Decision Trees, Naive Bayes Linear models: Linear Regression, Logistic Regression, Generalized Linear Models Support Vector Machines, Nonlinearity and Kernel Methods
Beyond Binary Classification: Multi-class/Structured Outputs, Ranking

UNIT–II
Unsupervised Learning Clustering: K-means/Kernel K-means Dimensionality Reduction: PCA and kernel PCA Matrix Factorization and Matrix Completion
Generative Models (mixture models and latent factor models)

UNIT–III
Evaluating Machine Learning algorithms and Model Selection: Introduction to Statistical Learning Theory, Ensemble Methods (Boosting, Bagging, Random Forests)

UNIT–IV
Biological foundations to intelligent Systems: Artificial Neural Networks.
Single layer and Multi layer Feed Forward NN, LMS and Back Propagation. Algorithm, Feedback networks and Radial Basis Function Networks

UNIT–V
Fuzzy Logic, Knowledge Representation and Inference Mechanism, Defuzzification Methods Fuzzy Neural Networks and some algorithms to learn the parameters of the network like GA

TEXT BOOKS:
1. Kevin Murphy, Machine Learning: A Probabilistic Perspective, MIT Press, 2012
2. Trevor Hastie, Robert Tibshirani, Jerome Friedman ,The Elements of Statistical Learning, Springer 2009 (freely available online)

REFERENCEBOOKS:
1. Christopher Bishop, Pattern Recognition and Machine Learning, Springer,2007.
2. J M Zurada," An Introduction to ANN", Jaico Publishing House
3. Simon Haykins, "Neural Networks" , Prentice Hall

COMPUTER VISION
(Professional Elective-1)

I-M.Tech I Semester **L T P C**
Course Code: B2ES103PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce students the fundamentals of image formation, major ideas, methods, and techniques of computer vision and pattern recognition
2. To develop an appreciation for various issues in the design of computer vision and object recognition systems
3. To provide the student with programming experience from implementing computer vision and object recognition application

COURSE OUTCOMES: At the end of this course, students will be able to
1. Study the image formation models and feature extraction for computer vision
2. Identify the segmentation and motion detection and estimation techniques
3. Develop small applications and detect the objects in various applications

UNIT–I
Image Formation Models Monocular imaging system , Orthographic & Perspective Projection ,Camera model and Camera calibration, Binocular imaging systems, Perspective, Binocular Stereopsis: Camera and Epipolar Geometry; Homography, Rectification, DLT, RANSAC, 3-D reconstruction frame work; Auto-calibration. Apparel, Binocular Stereopsis: Camera and Epipolar Geometry Homography, Rectification, DLT, RANSAC, 3-D reconstruction framework; Auto-calibration. Apparel, Stereovision

UNIT–II
Feature Extraction: Image representations (continuous and discrete) • Edge detection, Edge linking, corner detection, texture ,binary shape analysis, boundary pattern analysis, circle and ellipse detection, Light at Surfaces; Phong Model; Reflectance Map; Albedo estimation; Photometric Stereo; Use of Surface Smoothness Constraint; Shape from Texture, color, motion and edges.

UNIT–III
Shape Representation and Segmentation: Deformable curves and surfaces • Snakes and active contours Level set representations • Fourier and wavelet descriptors • Medial representations • Multi-resolution analysis, Region Growing, Edge Based approaches to segmentation, Graph-Cut, Mean-Shift, MRFs, Texture Segmentation

UNIT–IV
Motion Detection and Estimation • Regularization theory • Optical computation • Stereo Vision Motion estimation, Background Subtraction and Modelling, Optical Flow, KLT, Spatio -Temporal Analysis, Dynamic Stereo; Motion parameter estimation •Structure from motion, Motion Tracking in Video

UNIT–V
Object recognition • Hough transforms and other simple object recognition methods • Shape correspondence and shape matching •Principal component analysis• Shape priors for recognition

TEXT BOOKS:
1. D. Forsyth and J. Ponce, " Computer Vision – A modern approach" , 2nd Edition, Pearson Prentice Hall, 2012
2. Szeliski, Richard, "Computer Vision: Algorithms and Applications", 1st Edition, Springer - Verlag London Limited, 2011.
3. Richard Hartley and Andrew Zisserman, "Multiple View Geometry in Computer Vision", 2nd Edition, Cambridge University Press, 2004.

REFERENCE BOOKS:

1. K. Fukunaga, “Introduction to Statistical Pattern Recognition”, 2nd Edition, Morgan Kaufmann 1990.
2. Rafael C. Gonzalez and Richard E. Woods, “ Digital Image Processing”, 3rd Edition, Prentice Hall, 2008.
3. B. K. P. Horn, “Robot Vision”, 1st Edition, McGraw - Hill, 1986.
4. E.R. Davies “Computer and Machine Vision: Theory, Algorithms, Practicalities”, 4thEdition, Elsevier Inc, 2012.

COMMUNICATION BUSES AND INTERFACES
(Professional Elective-II)

I-M.Tech I Semester **L T P C**
Course Code:B2ES104PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce various serial inter falls and design applications.
2. To introduce CAN and PCI protocols.
3. To introduce developing of API for data transfer on serial bus.
4. To teach students design and development of peripherals to do data transfer

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data on to serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT–I
Serial Busses-Physical interface ,Data and Control signals, features ,limitations and applications of RS232, RS485, I^2C, SPI

UNIT–II
CAN-Architecture, Data transmission, Layers, Frame formats, applications

UNIT–III
PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT–IV
USB-Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT–V
Data Streaming Serial Communication Protocol-Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:
1. Jan Axelson, "Serial Port Complete COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson,"USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk,"PCI Express Technology", Mind share Press

REFERENCE BOOKS:
1. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copper hill Media Corporation, 2nd Edition, 2005.
2. Serial Front Panel Draft StandardVITA17.1 – 200x
3. Technical references on www.can-cia.org,www.pcisig.com,www.usb.org

PARALLEL PROCESSING
(Professional Elective-II)

I-M.Tech I Semester **LT P C**
Course Code:B2ES105PE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn the concept of parallel processing and implementation of pipelining.
2. To introduce up comingVLIW processor with case study of protocol applications.
3. To introduce multi threaded architecture and discuss various issues & performance protocols.
4. To familiarize with operating systems for multiprocessor system

COURSE OUTCOMES: At the end of this course, students will be able to
1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. Investigate issues related to compilers and instruction set based on type of architectures.

UNIT–I
Overview of Parallel Processing and Pipelining, Performance analysis, Scalability, Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques ,Software pipelining.

UNIT–II
VLIW processors: Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT–III
Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

UNIT–IV
Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

UNIT–V
Operating systems for multiprocessors systems Customizing applications on parallel processing platforms

TEXT BOOKS:
1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH

REFERENCE BOOKS:
1. V.Rajaraman , L.Sivaram Murthy, “Parallel Computers”,PHI.
2. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition
3. Kai Hwang, ZhiweiXu,“Scalable Parallel Computing”, MGH
4. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

ADVANCED COMPUTER ARCHITECTURE
(Professional Elective–II)

I-M.Tech I Semester **LT P C**
Course Code:B2ES106PE **3 0 0 3**

COURSE OBJECTIVES:
1. To make students know about the Parallelism concepts in Programming
2. To give the students an elaborate idea about the different memory systems and buses.
3. To introduce the advanced processor architectures to the students

COURSE OUTCOMES: At the end of this course, students will be able to
1. Understand pipelining, Instruction set architectures, memory addressing.
2. Understand multi threading by using ILP and supporting thread-level parallelism (TLP).
3. Solve Practical issues in inter connecting networks

UNIT–I
Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT–II
Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT–III
Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues-Hardware verses Software.

UNIT–IV
Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematics hared memory architecture, Distributed shared– memory architecture, Synchronization.

UNIT–V
Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in inter connecting networks, Examples of interconnection, Cluster, Designing of clusters.
Intel Architecture: Intel IA - 64IL Pin embedded and mobile markets Fallacies and pitfalls

TEXT BOOKS:
1. JohnL. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture – A Design Space Approach", Pearson Education

REFERENCE BOOKS:

1. John P.Shen and Miikko H. Lipasti, “Modern Processor Design: Fundamentals of Super Scalar Processors”, 2002, Beta Edition, McGraw - Hill.
2. Kai Hwang, aye A. Brigs., “Computer Architecture and Parallel Processing”, McGraw Hill.

DIGITAL SYSTEM DESIGN WITH FPGAS LAB

I-M.Tech I Semester **L T P C**
Course Code :B2ES104PC **0 0 4 2**

COURSE OBJECTIVES:

1. To understand HDL code for all gates
2. Able to write HDL code for Finite State Machine- Mealy and Moore Machines
3.To understand the design on FPGA kits

COURSE OUTCOMES:

1. To acquire knowledge of to write every code for digital circuits using HDL code
2. Able to small projects on FPGA/CPLD
3. To apply finite state machine- mealy and moore machines in Real time applications

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3styles.
8. Modelling of an Edge triggered and Level triggered FFs: D,SR,JK
9. Design of 4-bitbinary, BCD counters (synchronous / asynchronous reset) or any sequence counter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4-Bit Multiplier, Divider.
13. Design of ALU to Perform –ADD, SUB, AND-OR, 1’s and 2’s Compliment,
14. Implementing the above designs on FPGA kits.

SYSTEM DESIGN WITH EMBEDDED LINUX LAB

I-M.Tech I Semester **L T P C**
Course Code: B2ES105PC **0 0 4 2**

COURSE OBJECTIVES:

1. To understand and make effective use of Linux utilities and Shell scripting language(bash) to solve Problems.
2. To implement in C some standard Linux utilities such as ls, mv, cp etc. using system calls.
3. To develop the skills necessary for systems programming including file system programming, process and signal management, and inter process communication.

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Demonstrate the flashing OS on to the devices
2. Develop and interface the different devices like Arduino, Raspbery Pi, Beaglebone
3. Appreciate the necessity of Inter Process Communication and synchronization mechanisms
4. Apply the concept of hosting the website onboard and interfacing the USB webcam

LIST OF EXPERIMENTS:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable tex as instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity& automatically turn ON/OFF the high intensity LED's by taking some pre- defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Open wrt To the Device:** Attempt to use the device while connecting toa wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website (static / dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and there by host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course-I)

I-M.Tech I Semester **L T P C**
Course Code:B2ES101AC **2 0 0 0**

COURSE OBJECTIVES:
1. To improve student writing skills and level of readability
2. To learn about what to write in each section
3. To develop the student writing skills

COURSE OUTCOMES: At the end of the course students will be able to:
1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

UNIT–I
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT–II
Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Section sofa Paper, Abstracts Introduction

UNIT–III
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT–IV
key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT–V
Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first-time submission

TEXT BOOK:
1. Adrian Wall work, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London,20

REFERENCES BOOKS
1. Igh Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R(2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Hman N(1998),Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.

PEDAGOGY STUDIES
(Audit Course -I)

I-M.Tech I Semester **L T P C**
Course Code:B2ES102AC **2 0 0 0**

Pre requisite: None

COURSE OBJECTIVES: Students will be able to

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

COURSE OUTCOMES: Students will be able to understand:

1. What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT–I
Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT–II
Thematic overview: Pedagogical practices are being used by teachers informal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT–III
Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT–IV
Professional Development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT– V
Research gaps and future directions: Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

TEXT BOOK / REFERENCES BOOKS:
1. Ackers J, Hardman F (2001) Classroom interaction in Keny an primary schools,Compare,31(2):245-261.
2. Agrawal M(2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies,36 (3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana –does it count ? Multi-site teacher education research project (MUSTER) country report1. London: DFID

I- YEAR (II-SEMESTER)

ARM MICROCONTROLLERS

I-M.Tech II Semester	**L T P C**
Course Code: B2ES201PC	**3 0 0 3**

Prerequisite: Microprocessors and Microcontrollers

COURSE OBJECTIVES:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

COURSE OUTCOMES: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level tradeoff issues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT–I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions, nest vectored interrupt controller (NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT–II

Introduction to the ARM Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARM v5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT–III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT–IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4- specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT– V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU->FPCAR,FPU->FPDSCR, FPU -> MVFR0, FPU -> MVFR1. ARM Cortex - M4 and DSP

Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for theCortexM4-Biquadfilter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT-ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. JosephYiu, The Definitive Guide to ARM Cortex - M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - ARM System on Chip Architectures – Edison Wesley, 2000
2. David Seal-ARM Architecture Reference Manual, Edison Wesley, 2000.

DIGITAL CONTROL SYSTEMS

I-M.Tech II Semester **L T P C**
Course Code: B2ES202PC **3 0 0 3**

Prerequisite: Control Systems

COURSEOBJECTIVES:

1. To understand the fundamentals of digital control systems representations, z-transforms
2. To understand analysis of discrete complex domain: Z-Transforms
3. To understand the concepts of state variables analysis for discrete LTIV systems.
4. To understand the concepts of controllability and observability of discrete time systems
5. To get exposed the design aspects of controllers and for discrete time systems
6. To understand the concepts of the stability for discrete LTIV systems
7. To understand the design aspects of observers for discrete time systems.

COURSE OUTCOMES: At the end of this course, students will demonstrate the ability to

1. Obtain discrete representation of LTI systems.
2. Find the state space analysis of discrete time systems.
3. Test and analyze the controllability and observability for discrete time systems
4. Analyze stability of discrete time systems using various methods
5. Design and analyze digital controllers.
6. Design state feedback controllers and observers.

UNIT– I

Representation of Discrete time system: Basics of Digital Control Systems. Discrete representation of continuous systems. Sample and hold circuit. Mathematical Modeling of sample and hold circuit. Effects of Sampling and Quantization. Choice of sampling frequency. ZOH equivalent.

Z-Transforms, Mapping forms -plane to z plane, Properties of Z-Transforms and Inverse Z Transforms. Pulse Transfer function: Pulse transfer function of closed loop systems. Solution of Discrete time systems. Time response of discrete time system, Steady State errors.

UNIT-II

Discrete time state space analysis: State space representation of discrete time systems, Conversion of pulse transfer function to state space models and vice-versa, Solving discrete time state space equations, State Transition Matrix, Pulse Transfer Function Matrix. Discretization of continuous time state space equations. Concept of Controllability, stabilizability, observability, reach ability–Controllability and observability tests. Effect of pole zero cancellation on the controllability & observability.

UNIT-III

Stability analysis of discrete time system: Concept of stability in z-domain, Stability analysis discrete time system: by Jury test, using bilinear transformation. Stability Analysis of discrete time systems using Lyapunov methods.

UNIT-IV

Design of digital control system by conventional methods: Design and realization of digital PID Controller ,Design of discrete time controllers with bilinear transformation, Design of digital control system with dead beat response, Practical issues with dead beat response design.

UNIT-V

Design State Feedback Controllers And Observers :Design of discrete state feedback controllers through pole placement, Design of Discrete Observer for LTI System: Design of full order and reduced observers, Design of observer-based controllers.

TEXT BOOKS:

1. K. Ogata, “Digital Control Engineering”, Prentice Hall, Engle wood Cliffs, 1995.
2. M.Gopal, “Digital Control Engineering”, Wiley Eastern, 1988.
3. V. I .George and C.P. Kurian, Digital Control Systems, CENGAGE Learning, 2012

REFERENCE BOOKS:

1. G. F. Franklin, J. D. Powell and M .L. Workman, “Digital Control of Dynamic Systems”, Addison-Wesley, 1998.
2. B.C .Kuo, “Digital Control System ”, Holt, Rinehart and Winston, 1980.

IOT AND APPLICATIONS
(Professional Elective–III)

I-M.Tech II Semester **L T P C**
Course Code: B2ES207PE **3 0 0 3**

COURSE OBJECTIVES:

1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn about private implementation security issues in platform and design IOT application for industrial use.

COURSE OUTCOMES: At the end of this course, students will be able to

1. Understand the concept of IOT and M2M
2. Study IOT architecture and applications in various fields
3. Study IOT architecture and applications in various fields
4. Study the security and privacy issues in IOT.

UNIT–I

IoT& Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy &Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.

UNIT–II

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value
chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

UNIT–III

IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model- Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

UNIT–IV

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brown field IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IOT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, e Health.

UNIT–V

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues,

TEXT BOOKS:

1. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-on-Approach)”, 1st Edition, VPT, 2014.
2. Francis da Costa, “Rethinking the Internet of Things :A Scalable Approach to Connecting Everything”, 1st Edition, A press Publications, 2013.

REFERENCE BOOKS:

1. Cuno Pfister, “Getting Started with the Internet of Things”, Oreilly Media,2011.

VLSI SIGNAL PROCESSING
(Professional Elective-III)

I-M.Tech II Semester **L T P C**
Course Code: B2ES208PE **3 0 0 3**

COURSE OBJECTIVES:
1. To give knowledge about DSP algorithm.
2. To explain about retiming techniques, folding and register minimization path problem.
3. To introduce about algorithm strength reduction techniques &parallel processing of FIR and IIR filters.
4. To explain about finite word length effects and round off noise computation in DSP.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Ability to implement fast convolution algorithms.
4. Low power design aspects of processors for signal processing and wireless applications.

UNIT–I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits Representation of DSP algorithms Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power
Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT–II
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems
Unfolding-Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT–III
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT–IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution–Design of Fast Convolution algorithm by Inspection

UNIT–V
Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches
Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:
1. VLSI Digital Signal Processing-System Design and Implementation–Keshab K.Parthi, Wiley Inter Science, 1998.
2. VLSI and Modern Signal processing–Kung S.Y,H.J. While House,T.Kailath,PrenticeHall,1985.

REFERENCE BOOKS:
1. Design of Analog–Digital VLSI Circuits for Telecommunications and Signal Processing– Jose E.France, YannisTsividis, Prentice Hall, 1994.
2. VLSI Digital Signal Processing–Medisetti V.K, IEEE Press (NY), 1995.

SOC ARCHITECTURE
(Professional Elective-III)

I-M.Tech II Semester **L T P C**
Course Code:B2ES209PE **3 0 0 3**

COURSE OBJECTIVES:
1. To familiarize the basis of SOC design and its architectural issues.
2. To familiarize the design flow and verification of ASIP's and NISC's along with various design methodologies.
3. To introduce the functional simulation, synthesis, layout and timing analysis of single and multi-core systems.
4. To adapt the concept to voltage scaling & optimization of various design parameters on the basis of case studies.

COURSE OUTCOMES: At the end of this course, students will be able to
1. Understand the components of system, hardware and software.
2. Know the basic concepts of processor architecture and instructions.
3. Describe external and internal memory of SOC.
4. Get knowledge of bus models of SOC3.

UNIT–I
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT–II
Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT–III
Memory Design for **SOC:** Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor–memory interaction.

UNIT–IV
Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT–V
Application Studies / Case Studies**:** SOC Design approach, AES algorithms, Design and evaluation, Image compression–JPEG compression.

TEXT BOOKS:
1. Michael J. Flynn and Wayne Luk, "Computer System Design System – on - Chip", Wiley India Pvt. Ltd.
2. Steve Furber, "ARM System on Chip Architecture",2nd Edition, 2000, Addison Wesley Professional.

REFERENCE BOOKS:
1. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st Edition, 2004, Springer
2. Jason Andrews, "Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)", Newnes, BK and CDROM.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2001, Kluwer Academic Publishers.

HARDWARE SOFTWARE CO-DESIGN

I-M.Tech I Semester **L T P C**
Course Code:B2ES210PE **3 0 0 3**

COURSE OBJECTIVES:

1. To understand the design of mixed hardware-software systems.
2. To focus on common underlying modeling concepts, the design of hardware-software interfaces, and the trade-of between hardware and software components.
3. To understand Languages for System–Level Specification and Design

COURSE OUTCOMES: At the end of this course, students will be able to

1. Acquire the knowledge on various models
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools
4. Understand validation methods and adaptability.

UNIT–I

Co-Design Issues**:** Co-Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware–software partitioning distributed system co-synthesis

UNIT–II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architecturesfor High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT–III

Compilation Techniques and Tools for Embedded Processor Architectures**:** Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT–IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT–V

Languages for System–Level Specification and Design-I: System–level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosymasystem and lycossystem.

TEXT BOOKS:

1. Jorgen Staunstrup, “Hardware / Software Co- Design Principles and Practice”, Wayne Wolf – 2009,Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, “Hardware /Software Co-Design”, 2002, Kluwer Academic Publishers

REFERENCE BOOK:

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-design”, 2010, Springer

NETWORK SECURITY AND CRYPTOGRAPHY
(Professional Elective-IV)

I-M.Tech II Semester **L T P C**
Course Code:B2ES211PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce basic and advanced concepts of security.
2. To introduce various cryptography techniques.
3. To teach students various authentication techniques and to introduce various threats.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT–I
Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Crypt analysis of Classical Encryption Techniques.

UNIT–II
Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclide an Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT–III
Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT–IV
Public-Key(Asymmetric)Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT–V
Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection,PasswordManagement,Worms,viruses,Trojans,VirusCountermeasures,Firewalls,TrustedSystems.

TEXT BOOKS:
1. William Stallings, "Cryptography and Network Security ,Principle and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communicational Public World", Prentice Hall, 2ndEdition

REFERENCE BOOKS:
1. Christopher M.King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen North cutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher,2013.

PHYSICAL DESIGN AUTOMATION
(Professional Elective–IV)

I-M.Tech II Semester **L T P C**
Course Code:B2ES212PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce the physical design issues for VLSI automation.
2. To familiarize performance issues of VLSI circuits, various delay models &its estimation.
3. To introduce the placement &routing algorithms.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Study automation process for VLSI system design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process o f VLSI systems.

UNIT–I
Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT–II
Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT–III
Placement**:** Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT–IV
Global Routing**:** Problem formulation, classification of global routing, Maze routing algorithms, Line- Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.
Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT–V
Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing. Via Minimization: Constraint and Unconstrained via minimization.
Clock and Power Routing: Clocking schemes, design considerations for the clock ,Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:
1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani,3rdEd.,2005,
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, WILEY Student Edition, John Wileyons (Asia) Pvt. Ltd.

REFERENCE BOOKS:
1. Computer Aided Logical Design with Emphasis on VLSI–Hill & Peterson, 1993,Wiley.
2. Modern VLSI Design: Systems on silicon–Wayne Wolf, 2nded., 1998, Pearson Education Asia

ARM MICROCONTROLLERS LAB

I-M.Tech II Semester **L T P C**
Course Code: B2ES204PC **0 0 4 2**

COURSE OUTCOMES: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize toolsets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

COURSE OUTCOMES

1. Understand Temperature indication on an RGB LED
2. Understand the System clock real time alteration using the PLL modules.
3. Learn about Sample sound using a microphone and display sound levels on LEDs.

LIST OF ASSIGNMENTS:

Experiments to be carried out on Cortex-M3 development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

DIGITAL CONTROL SYSTEMS LAB

I-M.Tech II Semester **L T P C**
Course Code: B2ES205PC **0 0 4 2**

Perform the following experiments in real time by inter facing with the related hardware.

List of Experiments:

1. PWM pulse generation
2. Three phase voltage monitoring using A/D converter.
3. Three phase current monitoring using A/D converter.
4. Speed monitoring of AC motor.
5. Sine PWM pulse generation.
6. Inverter output voltage control.
7. Control of AC motor using UFD.
8. Control of DC motor using DC drive.

DISASTER MANAGMENT
(Audit Course -II)

I-M.Tech II Semester **L T P C**
Course Code:B2ES203AC **2 0 0 0**

COURSE OBJECTIVES:
1. To provide basic conceptual understanding of disasters and its relationships with development.
2. To gain understand approaches of Disaster Risk Reduction (DRR)
3. To maintain the relationship between vulnerability, disasters, disaster prevention and risk reduction.

COURSE OBJECTIVES: Students will be able to
1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches,
5. Planning and programming in different countries, particularly their home country or the countries they work in

UNIT–I
Introduction: Disaster: Definition, Factors and Significance, Difference between Hazard and Disaster, Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.
Disaster Prone Areas in India: Study of Seismic Zones, Areas Prone to Floods and Droughts, Landslides and Avalanches, Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami, Post-Disaster Diseases and Epidemics

UNIT–II
Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts**.**

UNIT–III
Disaster Preparedness and Management: Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT–IV
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT–V
Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India**.**

TEXT BOOKS:
1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal book Company.
2. Sahni, Pardeep Et.Al. (Eds.), "Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.

REFERENCE BOOKS:

1. Goel S.L., Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., NewDelhi.

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course-II)

I-M.Tech II Semester **L T P C**
Course Code: B2ES204AC **2 0 0 0**

PRE REQUISITE: None

COURSE OBJECTIVES:

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

COURSE OUTCOMES: Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students

UNIT-I

Neetisatakam - Holistic development of personality

- Verses-19,20,21,22(wisdom)
- Verses-29,31,32 (pride & heroism)
- Verses-26,28,63,65 (virtue)

UNIT-II

Neetisatakam –Holistic development of personality

- Verses-52,53,59 (dont's)
- Verses-71,73,75,78 (do's)

UNIT-III

Approach today to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses41,47,48,
- Chapter3-Verses13, 21,27, 35,Chapter 6-Verses5,13,17, 23,35,
- Chapter18-Verses 45, 46,48.

UNIT-IV

Statements of basic knowledge.

- Shrimad Bhagwad Geeta:Chapter2-Verses 56,62, 68
- Chapter 12-Verses13,14,15,16,17,18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT-V

- Chapter2-Verses17,Chapter 3-Verses 36,37,42,
- Chapter4-Verses 18, 38,39
- Chapter18–Verses 37,38,63

TEXT BOOKS / REFERENCES:

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

II- YEAR (I-SEMESTER)

SCRIPTING LANGUAGES
(Professional Elective–V)

II M. Tech I Semester **L T P C**
Course Code: B2ES313PE **3 0 0 3**

COURSE OBJECTIVES:

1. To explain the characteristics and uses of scripting languages.
2. To describe the various PERL concepts used in VLSI design.
3. To learn the concepts of TCL.
4. To Interpret Java Script, Python language, Python web system Design

COURSE OUTCOMES:
At the end of the course, students will be able to:

1. Understand the differences between typical scripting languages and typical system
2. Gain knowledge of the strengths and weakness of Perl, TCL, OOPS
3. Select an appropriate language for solving a given problem.
4. Acquire programming skills in scripting language

UNIT–I

Introduction to Scripts and Scripting: Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built- in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT–II

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT–III

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT–IV

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications' Internet-aware',' Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT–V

TK and Java Script: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript– Object models, Design Philosophy, Versions of Java Script, The JavaScript core language, Basic concepts of Python.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. David Barron, “The World of Scripting Languages”, Wiley Student Edition,2010.
2. Brent Welch, Ken Jones and Jeff Hobbs., “Practical Programming in Tcl and Tk”– 4thEdition, Prentice Hall
3. Herbert Schildt, “Java the Complete Reference”, 7th Edition,TMH.

REFERENCE BOOKS:

1. Clif Flynt, “Tcl/Tk: A Developer's Guide”,2003, Morgan Kaufmann Series.
2. John Ousterhout, “Tcl and the Tk Toolkit”, 2nd Edition, 2009, Kindel Edition.
3. Wojciech Kocjan and Piotr Beltowski, “Tcl8. 5Network Programming book”, Packt Publishing.
4. Bert Wheeler, “Tcl/Tk8.5 Programming Cookbook”, 2011, Packt Publishing Limited.

MEMORY TECHNOLOGIES
(Professional Elective–V)

II M.Tech I Semester **L T P C**
Course Code: B2ES314PE **3 0 0 3**

COURSE OBJECTIVES:
1. To introduce about various type of memory Architectures.
2. To introduce about various performance parameter of memory Architectures.
3. To introduce about various memory packing technologies.
4. To introduce about various 2D&3D memory Architectures

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Know, how of the state-of-the-art memory chip design

UNIT–I
Random Access Memory Technologies: Static Random-Access Memories (SRAMs), SRAM Cell Structures, MOSSRAM Architecture, MOSSRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT–II
DRAMs, MOSDRAM Cell, Bi CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers.

UNIT–III
Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT–IV
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT–V
Memory Hybrids (2D&3D),Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

TEXT BOOKS:
1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and aapplications”, Wiley Inter science
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition

REFERENCE BOOK:
1. Ashok K Sharma, ”Semiconductor Memories: Technology, Testing and Reliability, PHI

WIRELESS SENSOR NETWORKS
(Professional Elective–V)

II-M. Tech I Semester **L T P C**
Course Code: B2ES315PE **3 0 0 3**

COURSE OBJECTIVES:
1. To build understanding of the fundamental concepts of wireless communications and networks.
2. To learn mathematical modeling of a wireless communication channel.
3. To build basic concepts in designing transmitter and receiver of a wireless communication system.
4. To learn different wireless communication network standards.

COURSE OUTCOMES: Upon completion of the course, the student will be able to:
1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT–I
Introduction to Sensor Networks, unique constraints and challenges Advantage of Sensor Networks ,Applications of Sensor Networks, Types of wireless sensor networks

UNIT–II
Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT–III
Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol, IEEE 802.15.4standardandZigBee

UNIT–IV
Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion, Quality of a sensor network, Real-time traffic support and security protocols.

UNIT–V
Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to Tiny OS and nes C.

TEXT BOOKS:
1. Ad-Hoc Wireless Sensor Networks-C.Siva Ram Murthy, B.S.Manoj, Pearson
2. Principles of Wireless Networks– KavehPahLavenandP.KrishnaMurthy,2002,PE
3. Wireless Communication and Networking–WilliamStallings,2003, PHI.

REFERENCE BOOKS:
1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications – Andrea Goldsith, 2005 Cambridge University Press.
3. Mobile Cellular Communication - Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking - William Stallings, 2003, PHI.

ARTIFICIAL NEURAL NETWORKS
(Open Elective)

II M. Tech I Semester **L T P C**
Course Code: B2ES401OE **3 0 0 3**

COURSE OBJECTIVES:

2. To Survey of attractive applications of Artificial Neural Networks.
2. To practical approach for using Artificial Neural Networks in various technical, organizational and economic applications
3. To understand Associative Memories

COURSE OUTCOMES: At the end of the course, students will be able to:

1. To understand artificial neural network models and their training algorithms
2. To understand the concept of fuzzy logic system components,fuzzification and defuzzification
3. Applies the above concepts to real-world problems and applications.

UNIT–I

Introduction to Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrate and-Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.
Essentials of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application.

UNIT–II

Feed Forward Neural Networks: Single Layer Feed Forward Neural Networks: Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications.
Multilayer Feed forward Neural Networks: Credit Assignment Problem, Generalized Delta Rule, Derivation of Back propagation (BP) Training, Summary of Back propagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

UNIT–III

Associative Memories: Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associat or, Matrix Memories, Content Addressable Memory). Bidirectional Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM Stability Theorem. Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall Algorithm, Stability Analysis, Capacity of the Hop field Network.

UNIT–IV

Classical and Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

UNIT–V

Fuzzy Logic System: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods.

TEXT BOOKS:

1. Rajasekharan and Pai, Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications – PHI Publication.
2. Satish Kumar, Neural Networks,TMH,2004.

REFERENCE BOOKS:

1. James A Freeman and Davis Skapura, Neural Networks, Pearson Education, 2002.
2. Simon Hakins, Neural Networks, Pearson Education.
3. C. Eliasmith and Ch. Anderson, Neural Engineering, PHI.

INTERNET OF THINGS
(Open Elective)

II M. Tech I Semester **L T P C**
Course Code: B2ES402OE **3 0 0 3**

COURSE OBJECTIVES:
1. To learn IOT technology, security, standardization.
2. To learn IOT radiation, design principle.
3. To learn and design IOT application for industrial use.
4. To learn about private implementation security Isues in platform

COURSE OUTCOMES: At the end of the course, students will be able:
1. To introduce the terminology technology and its applications
2. To introduce the concept of M2M (machine to machine) with necessary protocols
3. To introduce the Python Scripting Language which issued in many IoT devices
4. To introduce the Raspberry PI platform, that is widely used in IoT applications
5. To introduce the implementation of web based services on IoT devices

UNIT–I
Introduction to Internet of Things–Definition and Characteristics of IoT, Physical Design of IoT–IoT Protocols, IoT communication models, Iot Communication APIs IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems, IoT Levels and Templates Domain Specific IoTs – Home, City, Environment, Energy, Retail, Logistics, Agriculture, Industry, health and Lifestyle

UNIT–II
IoT and M2M – Software defined networks, network function virtualization, difference between SDN and NFV for IoT Basics of IoT System Management with NETCOZF, YANG-NETCONF,YANG, SNMP NETOPEER

UNIT–III
Introduction to Python - Language features of Python, Data types, data structures, Control of flow, functions, modules, packaging, file handling, data/time operations, classes, Exception handling Python packages - JSON, XML, HTTP Lib, URLLib, SMTPLib

UNIT–IV
IoT Physical Devices and Endpoints - Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output, reading input from pins.

UNIT–V
IoT Physical Servers and Cloud Offerings – Introduction to Cloud Storage models and communication APIs Web server – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

TEXT BOOKS:
1. Internet of Things – Ahands - on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015, ISBN: 9788173719547
2. Getting Started with RaspberryPi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014, ISBN:9789350239759

REFERENCE BOOKS:
1. Francis da Costa, “Rethinking the Internet of Things: A Scalable Approach to Connecting Everything”,1st Edition, A press Publications, 2013.
2. Cuno P fister, “Getting Started with the Internet of Things”, O_ReillyMedia,2011

ADHOC AND SENSOR NETWORKS
(Open Elective)

II -M. Tech I Semester **L T P C**
Course Code: B2ES403OE **3 0 0 3**

COURSE OBJECTIVES:
1. To understand the different issues in Adhoc wireless network.
2. To analyze the design goals of routing protocol for Adhoc wireless network.
3. To learn about the different routing and transport layer protocols in adhoc wireless network.
4. To understand QoS and Energy management in Adhoc wireless network.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Student will understand the difference between Adhoc wireless and wireless network.
2. Student will implement MAC Protocol in Adhoc wireless networks.
3. Student will design routing protocol in Adhoc wireless networks.
4. Student will implement QoS and energy management in Adhoc wireless network

UNIT–I
Introduction: Fundamentals of Wireless Communication Technology – The Electromagnetic Spectrum – Radio propagation Mechanisms –Characteristics of the Wireless Channel-mobile adhoc networks (MANETs) and wireless sensor networks (WSNs): concepts and architectures. Applications of AdHoc and Sensor networks, Design Challenges in Adhoc and Sensor Networks.

UNIT–II
MAC Protocols for adhoc wireless networks: Issues in designing a MAC Protocol- Classification of MAC Protocols- Contention based protocols-Contention based protocols with Reservation Mechanisms- Contention based protocols with Scheduling Mechanisms –Multichannel MAC-IEEE 802.11

UNIT–III
Routing Protocols And Transport Layer In Ad Hoc wireless networks: Issues in designing a routing and Transport Layer protocol for Ad hoc networks- proactive routing, reactive routing (on-demand), hybrid routing-Classification of Transport Layer solutions-TCP over Ad hoc wireless Networks.

UNIT–IV
Wireless Sensor Networks (WSNs)and MAC Protocols: Single node architecture: hardware and software components of a sensor node – WSN Network architecture: typical network architectures-data relaying and aggregation strategies -MAC layer protocols: self-organizing, Hybrid TDMA/FDMA and CSMA based MAC-IEEE 802.15.4.

UNIT–V
WSN routing, Localization & QoS: Issues in WSN routing – OLSR- Localization – Indoor and Sensor Network Localization-absolute and relative localization, triangulation – QOS in WSN – Energy Efficient Design-Synchronization-Transport Layer issues

TEXT BOOKS:
1. C. Siva Ram Murthy, and B.S.Manoj, “AdHoc Wireless Networks: Architectures and Protocols”, Prentice Hall Professional Technical Reference, 2008.
2. Kazem Sohraby, Daniel Minoli, &Taieb Znati, “Wireless Sensor Networks-Technology, Protocols, and Applications”, John Wiley, 2007
3. Anna Hac, “Wireless Sensor Network Designs”, John Wiley, 2003.

REFERENCE BOOKS:
1. Carlos De Morais Cordeiro, Dharma Prakash Agrawal “AdHoc & Sensor Networks: Theory and Applications”, World Scientific Publishing Company, 2006.
2. Feng Zhao and Leonides Guibas,“ Wireless Sensor Networks”, Elsevier Publication –2002.
3. Holger Karl and And reas Willig “Protocols and Architectures for Wireless Sensor Networks”, Wiley, 2005

INFORMATION RETRIEVAL SYSTEMS
(Open Elective)

II-M.Tech I Semester **L T P C**
Course Code:B2ES404OE **3 0 0 3**

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Use different information retrieval techniques in various application areas
2. Apply IR principles to locate relevant information large collections of data
3. Analyze performance of retrieval systems when dealing with unmanaged data sources
4. Implement retrieval systems for web search tasks.

COURSE OUTCOMES: At the end of the course, students will be able to:
1. Use different information retrieval techniques in various application areas
2. Apply IR principles to locate relevant information large collections of data
3. Analyze performance of retrieval systems when dealing with unmanaged data sources
4. Implement retrieval systems for web search tasks.

UNIT–I
Boolean retrieval. The term vocabulary and postings lists. Dictionaries and tolerant retrieval. Index construction. Index compression

UNIT–II
Scoring, term weighting, and the vector space model. Computing cores in a complete search system. Evaluation in information retrieval Relevance Feedback and query expansion

UNIT–III
XML retrieval. Probabilistic information retrieval. Language models for information retrieval. Text classification. Vector space classification

UNIT–IV
Support vector machines and machine learning on documents, Flat clustering, Hierarchical clustering, Matrix decompositions and latent semantic indexing.

UNIT–V
Web search basics. Web crawling and indexes, Link analysis

TEXT BOOKS:
1. Introduction to Information Retrieval, Christopher D.Manning and Prabhakar Raghavan and Hinrich Schütze, Cambridge University Press, 2008.

REFERENCE BOOKS:
1. Information Storage and Retrieval Systems: Theory and Implementation, Kowalski, Gerald, Mark T Maybury, Springer.
2. Modern Information Retrieval, Ricardo Baeza -Yates, Pearson Education, 2007
3. Information Retrieval: Algorithms and Heuristics, David A Grossman and Ophir Frieder, 2nd edition, Springer, 2004.
4. Information Storage & Retieval, Robert Korfhage, John Wiley, & Sons.

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